ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURE WITH SYMMETRICAL POSITIVE AND NEGATIVE ESD PROTECTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to semiconductor circuit structures, and in particular, to semiconductor circuit structures providing electrostatic discharge (ESD) protection for integrated circuits.

2. Description of the Related Art

[0002] Electrostatic discharge (ESD) protection devices are widely used in an integrated circuit (IC) to protect the electronic devices within the IC, e.g., bipolar junction transistors (BJTs) and metal oxide semiconductor field effect transistors (MOSFETs), from spurious voltage pulses caused by various sources of electrostatic energy. Numerous conventional ESD protection structures and devices are well known in the art, and include the use of BJTs, MOSFETs, grounded gate metal oxide semiconductor (GGMOS) structures, low voltage triggered silicon controlled rectifiers (LVTSCRs), triacs and diacs.

[0003] Electrostatic discharge events produce voltages that typically have large magnitudes and can be either positive or negative in polarity (i.e., with respect to the reference, or ground, potential of the circuit to be protected). Most conventional ESD protection structures can only protect against ESD events of a single polarity. Accordingly, for protection against both positive and negative ESD voltages, at least two distinct ESD protection structures are normally required.

[0004] For some applications, as a practical matter, only one dedicated ESD protection structure need be provided for protecting against positive ESD event voltages. Negative ESD event voltages can be clamped at a safe voltage by the inherent body diode present in most circuits (discussed in more detail below).

[0005] Referring to Figure 1, one common device used for an ESD protection structure is a diac 10, which is well known in the art. Between the two electrical terminals 11a (T1), 11b (T2) multiple semiconductor layers 12p, 12n, 14, 16n, 16p. As is well known, the diac 10 is a bi-directional device that becomes conductive when the voltage at one terminal T1 (T2) becomes more positive than the voltage at the other terminal T2 (T1) by an amount greater than the predetermined trigger voltage, and remains conductive, i.e., continues to conduct current from the more positive to the less positive terminal, until such inter-terminal voltage becomes less than a predetermined holding voltage.

[0006] Referring to Figure 2, the implementation of a diac 10a as an ESD protection structure within an IC environment typically appears as shown. The P-type substrate 14, which is typically connected to a circuit reference, or ground, electrode 18, has two N-type wells 12n, 16n diffused or implanted into its surface, separated by a gap region 14g. Within the first well 12n are a similarly diffused or implanted N-type contact region 12na and P-type contact region 12p both of which are connected to one of the diac terminals 11a. Within the second well 16n are another similarly diffused or implanted N-type contact region 16na and P-type contact region 16p, both of which are connected to the other diac terminal 11b. As noted above, this diac structure 10a will provide protection for a positive voltage appearing across the terminals 11a,

11b (one of which is typically connected to the circuit reference electrode 18), but will not provide the primary protection against negative ESD voltages due to the so-called "body diode" which exists by nature of the PN junction between the P-type substrate 14 and the N-type well 12n/16n.

[0007] For many circuits or applications, such asymmetrical ESD protection can be acceptable. However, some circuits or systems must be tolerant of negative voltages appearing at the terminals to be protected from ESD events without being clamped at the typically low voltages associated with the body diode. One example of such a circuit would be a circuit used for measuring current in the operation of a circuit or system with a heavy inductive load (e.g., for driving a motor). For proper accuracy, influences created by the chip during operation of the host circuit or system must be minimized, including avoidance of premature voltage clamping caused by voltage spikes which may at first appear, albeit incorrectly, to be an ESD event.

SUMMARY OF THE INVENTION

[0008] In accordance with the presently claimed invention, an electrostatic discharge (ESD) protection structure is provided with a diac in which substantially similar ESD protection is provided for both positive and negative ESD voltages appearing at the circuit electrode sought to be protected.

[0009] In accordance with one embodiment of the presently claimed invention, an electrostatic discharge (ESD) protection structure with a diac includes one or more reference electrodes, a circuit electrode, a semiconductor material, semiconductor regions and

semiconductor wells. The semiconductor material is of a first conductivity type and in electrical communication with one or more of the one or more reference electrodes. A first semiconductor region of the first conductivity type is disposed on the semiconductor material and in electrical communication with at least one of the one or more reference electrodes. A second semiconductor region of a second conductivity type is disposed on the semiconductor material proximate the first semiconductor region and in electrical communication with the at least one of the one or more reference electrodes. A first semiconductor well of the second conductivity type is disposed in the semiconductor material. A second semiconductor well of the first conductivity type is disposed in the first semiconductor well. A third semiconductor region of the first conductivity type is disposed on the second semiconductor well and in electrical communication with the circuit electrode. A fourth semiconductor region of the second conductivity type is disposed on the second semiconductor well and in electrical communication with the circuit electrode.

[00010] In accordance with another embodiment of the presently claimed invention, an electrostatic discharge (ESD) protection structure with a diac includes one or more reference electrodes, a circuit electrode, a semiconductor material, semiconductor regions and semiconductor wells. The semiconductor material is of a first conductivity type and in electrical communication with one or more of the one or more reference electrodes. A first semiconductor region of the first conductivity type is disposed on the semiconductor material and in electrical communication with at least one of the one or more reference electrodes. A second semiconductor region of the second conductivity type is disposed on the semiconductor material

proximate the first semiconductor region and in electrical communication with the at least one of the one or more reference electrodes. A first semiconductor well of a second conductivity type is disposed in the semiconductor material. A second semiconductor well of the second conductivity type is disposed in the first semiconductor well. A third semiconductor well of the first conductivity type is disposed in the second semiconductor well. A third semiconductor region of the first conductivity type is disposed on the third semiconductor well and in electrical communication with the circuit electrode. A fourth semiconductor region of the second conductivity type is disposed on the third semiconductor well and in electrical communication with the circuit electrode.

[00011] In accordance with still another embodiment of the presently claimed invention, an electrostatic discharge (ESD) protection structure with a diac includes one or more reference electrodes, a circuit electrode, a semiconductor material, a semiconductor layer, semiconductor regions and semiconductor wells. The semiconductor material is of a first conductivity type and in electrical communication with one or more of the one or more reference electrodes. A first semiconductor region of the first conductivity type is disposed on the semiconductor material and in electrical communication with at least one of the one or more reference electrodes. A second semiconductor region of the second conductivity type is disposed on the semiconductor material proximate the first semiconductor region and in electrical communication with the at least one of the one or more reference electrodes. The semiconductor layer is of a second conductivity type and disposed in the semiconductor material. A first semiconductor well of the second conductivity type is disposed on the semiconductor layer. A second semiconductor well

of the first conductivity type is disposed in the first semiconductor well. A third semiconductor region of the first conductivity type is disposed on the second semiconductor well and in electrical communication with the circuit electrode. A fourth semiconductor region of the second conductivity type is disposed on the second semiconductor well and in electrical communication with the circuit electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[00012] Figure 1 depicts the structure of a conventional diac.

[00013] Figure 2 is a cross-sectional view of a conventional implementation of a diac in an IC.

[00014] Figures 3A is a cross-sectional view of an implementation of a diac structure for ESD protection in accordance with one embodiment of the presently claimed invention.

[00015] Figures 3B is a cross-sectional view of an implementation of a diac structure for ESD protection in accordance with another embodiment of the presently claimed invention.

[00016] Figure 4 is a graph of the current-versus-voltage characteristic for one example implementation of a diac structure for ESD protection in accordance with the presently claimed invention.

DETAILED DESCRIPTION OF THE INVENTION

[00017] The following detailed description is of example embodiments of the presently claimed invention with references to the accompanying drawings. Such description is intended to be illustrative and not limiting with respect to the scope of the present invention. Such embodiments are described in sufficient detail to enable one of ordinary skill in the art to practice the subject invention, and it will be understood that other embodiments may be practiced with some variations without departing from the spirit or scope of the subject invention.

[00018] Throughout the present disclosure, absent a clear indication to the contrary from the context, it will be understood that individual circuit elements as described may be singular or plural in number. For example, the terms "circuit" and "circuitry" may include either a single component or a plurality of components, which are either active and/or passive and are connected or otherwise coupled together (e.g., as one or more integrated circuit chips) to provide the described function. Additionally, the term "signal" may refer to one or more currents, one or more voltages, or a data signal. Within the drawings, like or related elements will have like or related alpha, numeric or alphanumeric designators.

[00019] Referring to Figure 3A, in accordance with one embodiment of the presently claimed invention, an ESD protection structure 100a includes a diac and can be described as follows. (It should be understood that while the following discussion is in terms of specific orders or sequences of P-type and N-type semiconductor materials, substrates, layers, wells, diffusions or implants, such orders or sequences can be reversed, i.e., P-types and N-types can be interchanged, in accordance with well known IC design and fabrication techniques without departing from the spirit and scope of the presently claimed invention. Further, it should also be

understood that the semiconductor layers, wells, and regions discussed herein can be implemented using well known diffusion and implantation techniques as appropriate.)

[00020] A P-type substrate 114 includes an N-type region 112 which can be implemented as an N-type well, or alternatively as an N-type isolation layer 112ni on top of which is an N-type well 112nw. (It should be understood that the substrate 114 can include all of the P-type semiconductor material as shown, or alternatively, can be a P-type substrate area 114s on top of which the remaining semiconductor layers and regions are deposited or otherwise added.) Within this well 112/112nw is a P-type well 112pw. In turn, within this well 112pw are an N-type contact region 112na and a P-type contact region 112pa, both of which are connected to a circuit electrode 111a for the circuit sought to be protected against ESD events. As a result, two blocking junctions are provided between the circuit electrode 111a and the reference electrode 118 to which the substrate 114 is connected: the PN junction between wells 112pw and 112/112nw; and the PN junction between well 112/112nw and substrate 114/114s.

[00021] The substrate 114/114s includes at least one additional set of contact regions, including one or more of: an N-type contact region 116na and a P-type contact region 116pa connected to a circuit reference electrode 111ba; and another N-type contact region 116nb and P-type contact region 116pb connected to another circuit reference terminal 111bb. These N-type contact regions 116na, 116nb and P-type contact regions 116pa, 116pb can be distinct contact regions, or alternatively, can form common N-type and P-type semiconductor rings within an annular region about the N-type well 112/112nw. Additionally, the reference electrodes 111ba, 111bb can be separate electrodes or one common electrode connected or available for connection

to the reference electrode 118 to which the substrate 114/114s is connected. Additionally, these contact regions 116na, 116pa, 116nb, 116pb can, in turn, be disposed within respective P-type wells 114wa, 114wb within the substrate 114/114s, with such wells 114wa, 114wb being either distinct wells or portions of a common annular well (e.g., a latch-up guard ring) about N-type well 112/112nw.

[00022] Referring to Figure 3B, an alternative embodiment 100b of an ESD protection structure with a diac in accordance with the presently claimed invention includes a structure similar to that shown in and described in connection with Figure 3A. In this embodiment 100b, the contact regions 116n, 116p for the reference electrode 111b are disposed between wells 112a/112nwa, 112pwa, 112b/112nwb, 112pwb and contact regions 112naa, 112paa, 112nab, 112pab for the circuit electrodes 111aa, 111ab. Similar to the embodiment 100a of Figure 3A, these outer semiconductor wells 112a/112nwa, 112pwa, 112b/112nwb, 112pwb and contact regions 112naa, 112paa, 112nab, 112pab can be separate or portions of an annular region surrounding the contact regions 116n, 116p for the reference electrode 111b.

[00023] As is well known in the art, the various semiconductor layers, wells and contact regions discussed above will have various concentrations of dopants introduced to change or otherwise control the charge carrier concentrations. Further, also in accordance with well known semiconductor circuit fabrication techniques, the dopant concentrations of the P-type contact regions 112pa, 116pa, 116pb, 112paa, 112pab, 116p will generally be greater than the dopant concentrations for the P-type wells 112pw, 114wa, 114wb, 112pwa, 112pwb, 114w and substrate 114/114s. Similarly, the dopant concentrations for the N-type contact regions 112na, 116na,

116nb, 112naa, 112nab, 116n will be greater than the dopant concentrations of the N-type wells 112/112nw and isolation layer 112ni.

[00024] Operations of these ESD protection structures 100a, 100b during ESD events are in accordance with well-known operating principles for such diac structures and need not be discussed here. (For example, for discussions about general principles of operation of these types of ESD protection structures, including current avalanche breakdown mechanisms and "double injection" of holes and electrons during ESD events, see U.S. Patent Nos. 6,355,959, 6,433,368 and 6,541,801, the disclosures of which are incorporated herein by reference.)

[00025] Referring to Figure 4, by eliminating the normal body diode effect through the introduction of the dual blocking junctions (discussed above), the ESD protection provided by the above-described ESD protection structures 100a, 100b becomes substantially symmetrical with respect to positive and negative polarity ESD voltages. As can be seen, for both positive and negative voltage biases at the circuit electrodes 111a, 111aa, 111ab, voltage breakdown pursuant to the desired ESD protection occurs at approximately 30 volts in both cases. Accordingly, an ESD protection structure with a diac in accordance with the presently claimed invention provides substantially similar ESD protection for both positive and negative ESD voltages appearing at the circuit electrode sought to be protected.

[00026] Various other modifications and alternations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and the spirit of the invention. Although the invention has been described in connection

with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.